What is claimed :

1. A method for conducting an alternative bit line stress test on a flash memory device, the method comprising:

applying activation signals to select transistors to selectively couple global bit lines to associated local bit lines, wherein adjacent local bit lines are selectively coupled to different global bit lines; and

applying potential voltage differences across adjacent global bit lines.

2. The method of claim 1 wherein resulting voltage potentials across adjacent local bit lines are different.

3. A method for conducting an alternative bit line stress test on a flash memory device, the method comprising:

selectively coupling a first local bit line to a first global bit line;

selectively coupling a second local bit line to a second global bit line;

selectively coupling a third local bit line to the first global bit line;

selectively coupling a fourth local bit line to the second global bit line; and

applying a voltage potential across the first and second global bit lines.

4. The method of claim 3 wherein there is a voltage potential difference across adjacent local bit lines as the result of applying the voltage potential across the first and second global bit lines.

5. The method of claim 3 wherein the local bit lines are sequentially positioned adjacent each other.

6. The method of claim 3 wherein the flash memory device is a floating gate memory device.

7. A method for conducting an alternative bit line stress test on a memory array of a flash memory device, the method comprising:

programming a group of memory cells of the flash memory with alternating logic states;

selectively coupling even local bit lines to a first global bit line;

selectively coupling odd local bit lines to a second global bit line;

monitoring the first and second global bit lines; and

indicating a short condition when a monitored state of either the first or the second bit lines is different than a state programmed into a first memory cell of the group of memory cells.

8. The method of claim 7 wherein select transistors are coupled between the local bit lines and the global bit lines.

9. The method of claim 7 wherein selectively coupling odd local bit lines comprises coupling a first group of alternating local bit lines to the first global bit line and selectively coupling even local bit lines comprises coupling a second group of alternating local bit lines to the second global bit line.

10. The method of claim 7 wherein selectively coupling odd local bit lines comprises activating a first select transistor that is coupled between a first even local bit line and a first even global bit line.

11. The method of claim 7 wherein selectively coupling comprises:

generating an activation signal coupled to a control gate of a select transistor; and

the select transistor coupling a first even local bit line to a first even global bit line in response to the activation signal.

12. The method of claim 7 wherein selectively coupling comprises:

generating a plurality of activation signals, each signal coupled to a different select transistor of a plurality of select transistors; and

the plurality of select transistors selectively coupling the even local bit lines to the even global bit lines and the odd local bit lines to the odd global bit lines in response to the activation signals.

13. The method of claim 7 wherein the integrated circuit memory is a floating gate flash memory device.

14. The method of claim 7 wherein the alternating logic states comprises alternating logic high and low states.

15. The method of claim 14 wherein the memory array is a floating gate memory array and the alternating logical high and low states are comprised of a charge and a lack of charge on the floating gate.